

EE2071 Micro electronic workshop:

Gate level systolic multiplier



Example of chip to implement our multiplier

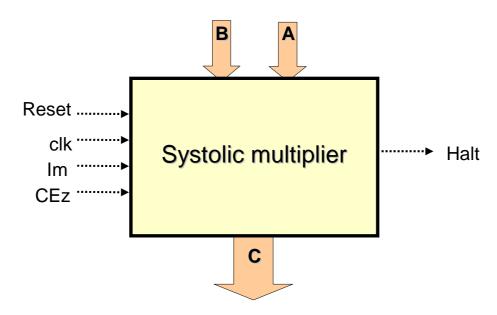
0 <u>Purpose</u>

This laboratory report is our introduction to the principle of manual synthesis for a digital system. We will try to reproduce a design from Verilog Hardware Description Language (in Register Transfer Level) simulated with the Cadence Simucad Silos software to a graphical gate level using Altera Maxplus. We are going to meet this challenge by designing a systolic multiplier with two 8bits inputs and a 16bits output. This multiplier is designed for a digital signal processor and has thus to be able to load 2 input and keep 1 to multiply different values to it.

In a first time we are going to show bloc by bloc the internal components of our design and in a second time we are going to implement the gate level equivalent by reproducing the same behaviour of these components.

1 <u>Verilog multiplier</u>

First of all, let's see how this component is interfaced:



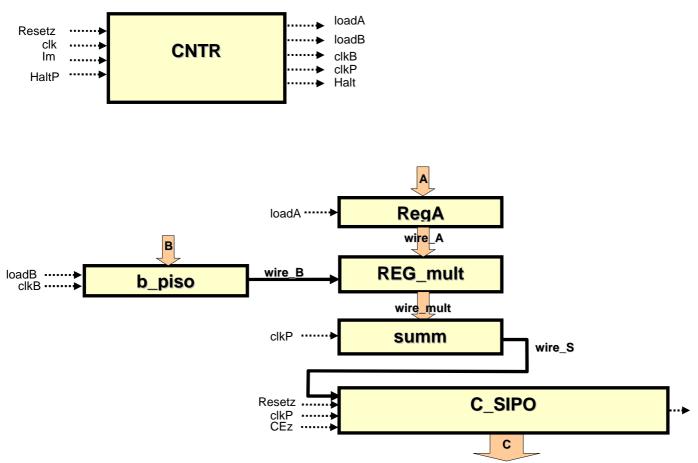
Details:

As said previously, A and B are on 8 bits, C is on 16 bits

The signal Im (Input mode) allows selecting if we want to load 1 or 2 inputs (A is not loaded if Im = 0). The output C is in high impedance state when CEz = 1.

The output Halt is set when the multiplier has completely finished its calculation and is thus ready.

Internal components



Verilog codes:

The 3 next components were quite straight forward, I thus detail them too much.

🗏 regA.v	
1	<pre>module regA(wire_A , A,loadA);</pre>
2	output [7:0] wire_A;
3	input [7:0] A;
4	input loadA;
5	reg [7:0] wire_A;
6	
7	always@(negedge loadA)
8	wire_A = A;
9	
	endmodule

🖹 b_piso.v	
1	<pre>module b_piso(wire_B, B,loadB,c1kB);</pre>
2	output wire_B;
3	reg wire_B;
4	input [7:0] B;
5	<pre>input loadB, clkB;</pre>
6	reg [7:0] B_reg;
7	
8	
9	always@(negedge loadB) begin
10	B_reg = B;
11	<pre>wire_B = B_reg[0];</pre>
12	end
13	always@(pacadae_allyD)_basin
14	always@(posedge clkB) begin
16	B_reg[6:0] = B_reg[7:1];
10	<pre>wire_B = B_reg[0]; end</pre>
18	enu
10	endmodule

REG_mult.v	
1	<pre>module REG_mult(wire_mult, wire_A, wire_B);</pre>
2	<pre>output [7:0] wire_mult;</pre>
3	<pre>input [7:0] wire_A;</pre>
4	input wire_B;
5	<pre>reg [7:0] wire_mult;</pre>
6	
7	always @ (wire_B or wire_A)
8	wire_mult = wire_B * wire_A;
9	
	endmodule

In the beginning, I designed a really simple RTL multiplier, but I never succeeded to make it work, I still don't know why. I thus decided to start again and I did it in the same principle than the gate level one:

=> It's composed by an adder block (a specialised full adder) where the carry out is fed back in the carry in at the next clock pulse. This is a implicit way to ripple it quickly and efficiently.

adder_block	.v 🔲 🖂 🛛
1	<pre>module adder_block(So , mult,Si,Resetz,clkP);</pre>
2	output So;
3	input mult, Si, Resetz, clkP;
4	reg carry, So;
5	
6	always@(negedge Resetz) begin
7	carry = 0;
8	So = 0;
9	end
10	
11	always@(posedge clkP) if(Resetz)
12	<pre>{carry, So} = Si + mult + carry;</pre>
13	-
	endmodule

...and a module that instantiate it 8 times:

🗉 summ.v	
1	<pre>module summ(wire_S , mult,Resetz,clkP);</pre>
2	output wire_S;
3	<pre>input [7:0]mult;</pre>
4	input Resetz, clkP;
5	wire [6:0]S_int;
6	
7	<pre>adder_block INST0(wire_S, mult[0], S_int[0], Resetz, clkP);</pre>
8	<pre>adder_block INST1(S_int[0], mult[1], S_int[1], Resetz, clkP);</pre>
9	<pre>adder_block INST2(S_int[1], mult[2], S_int[2], Resetz, clkP);</pre>
10	adder_block INST3(S_int[2], mult[3], S_int[3], Resetz, clkP);
11	adder_block INST4(S_int[3], mult[4], S_int[4], Resetz, clkP);
12	<pre>adder_block INST5(S_int[4], mult[5], S_int[5], Resetz, clkP);</pre>
13	<pre>adder_block INST6(S_int[5], mult[6], S_int[6], Resetz, clkP);</pre>
14	<pre>adder_block INST7(S_int[6], mult[7], S_int[6], Resetz, clkP);</pre>
15	
	endmodule

C_SIPO.v	
1	<pre>module C_SIPO(C , HaltP,wire_S,Resetz,CEz,clkP);</pre>
2 3	output [15:0]C; output HaltP;
4	input wire S, clkP, Resetz, CEz;
5	req [15:0] C, reqC;
ó	reg HaltP;
7	to the task is a first of the task of task
8	initial begin reqC = 0;
10	C = 0;
11	HaltP = 0;
12	end
13	
14 15	always@(negedge Resetz)
16	HaltP = 0;
17	end
18	
19	always@(posedge clkP)
20 21	if(Resetz)
22	#1 reqC[15] = wire S;
23	HaltP = reqC[0];
24	end
25	
26 27	always@(CEz or regC) begin if(!CEz)
28	C = reqC;
29	else
30	C = 16'hzzzz;
31	end
32	endmodule

CNTR.v		
1	<pre>module CNTR(loadA, loadB, cez, clkP, Halt, clkB,</pre>	//outputs
2	Im, clk, CEz, Resetz, HaltP);	//inputs
3		
4	output loadA, loadB, cez, clkP, Halt, clkB;	
5	<pre>input clk, Resetz, Im, CEz, HaltP;</pre>	
6	<pre>reg Halt, halt_tmp;</pre>	
7	and an load A Bracks of Ta	
8	assign loadA = Resetz * Im,	
10	loadB = Resetz, clkP = ~Halt * clk,	
11	clkB = ~clk,	
12	cez = CEz:	
13	,	
14	initial begin	
15	Halt = 0;	
16	halt_tmp = 0;	
17	end	
18		
19		
20	always@(negedge Resetz) Halt = 0;	
21	always@(posedge clkP) halt_tmp = HaltP; always@(posedge clkP) Halt = balt tmp;	
22 23	always@(negedge clkP) Halt = halt_tmp;	
23		
27	endmodule	

Instantiation of all the components:

Ē	Systolic_	_multiplier.v
	1	<pre>module Systolic_multiplier(C,Halt , A,B,Im,Resetz,CEz,clk);</pre>
	2	input Im, clk, CEz, Resetz;
	3	input [7:0] A, B;
	4	output [15:0] C; output Halt;
	6	wire loadA, loadB, cez, clkP, clkB, HaltP, wire B, So;
	7	wire [7:0] wire_A, wire_mult;
	8	
	9	CNTR inst1(loadA,loadB,cez,clkP, Halt,clkB, // outputs
	10 11	Im,clk,CEz,Resetz,HaltP); // inputs
	12	regA inst2(wire_A , A,loadA);
	13	
	14	b_piso inst3(wire_B , B,loadB,clkB);
	15 16	DEC mult insth/wiwe mult wiwe A wiwe D).
	17	REG_mult inst4(wire_mult , wire_A,wire_B);
	18	<pre>summ inst5(So , wire_mult,Resetz,clkP);</pre>
	19	
	20	C_SIPO inst6(C,HaltP , So,Resetz,cez,clkP); endmodule

testfile: (this test file is simplified to be able monitoring the output in the result text file, see next page)

<pre>imodule Systolic_multiplier_test; reg [7:0] A, B; reg Im,Resetz,CEz,Clk; wire [15:0] C; wire Halt; Systolic_multiplier inst(C, Halt, A, B, Im, Resetz, CEz, clk); initial begin initial begin i</pre>	×
<pre>reg Im,Rēsetz,CEz,CEk; wire [15:0] C; wire Halt; Systolic_multiplier inst(C, Halt, A, B, Im, Resetz, CEz, clk); initial begin %monitor(\$time, " clk = %b, C = %b, Halt = %b", clk, C, Halt); clk = 0; If Im = 1; CEz = 0; Resetz = 1; A = -127; // result expected : 3F01 #1 Resetz = 0; #1 Resetz = 1; wait(Halt); Im = 0; B = -127; // result expected : C0FF #1 Resetz = 1; wait(Halt); Im = 1; A = -127; // result expected : C0FF #1 Resetz = 1; wait(Halt); Im = 1; A = -127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 1; wait(Halt); Im = 1; A = 127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 1; wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 1; wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; Wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; Wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; Wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; Wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; Wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; Wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; Wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; Wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; Wait(Halt); A = 127; // result expected : C0FF #1 Resetz = 1; Wait(Halt); A = 127; // result expected : C0FF A = 127;</pre>	^
<pre>wire [15:0] C; wire Halt; Systolic_multiplier inst(C, Halt, A, B, Im, Resetz, CEz, clk); initial begin \$monitor(\$time, " clk = %b, C = %b, Halt = %b", clk, C, Halt); Clk = 0; Im = 1; CEz = 0; Resetz = 1; A = -127; B = -127; // result expected : 3F01 #1 Resetz = 0; #1 Resetz = 1; wait(Halt); Im = 0; B = 127; // result expected : C0FF #1 Resetz = 1; wait(Halt); Im = 1; A = 127; // result expected : C0FF #1 Resetz = 1; wait(Halt); Im = 1; A = 127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 1; wait(Halt); Second Second Seco</pre>	
<pre>5</pre>	
<pre> wire Halt; Systolic_multiplier inst(C, Halt, A, B, Im, Resetz, CEz, clk); initial begin \$monitor(\$time, " clk = %b, C = %b, Halt = %b", clk, C, Halt);</pre>	
<pre>Systolic_multiplier inst(C, Halt, A, B, Im, Resetz, CEz, clk); initial begin \$monitor(\$time, " clk = %b, C = %b, Halt = %b", clk, C, Halt); Clk = 0; Im = 1; CEz = 0; Resetz = 1; A = -127; B = -127; // result expected : 3F01 #1 Resetz = 0; #1 Resetz = 1; wait(Halt); Im = 0; B = -127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 1; wait(Halt); Im = 1; A = 127; B = -127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 1; wait(Halt);</pre>	
<pre>Systolic_multiplier inst(C, Halt, A, B, Im, Resetz, CEz, clk); initial begin (notice for the second se</pre>	
<pre>9 10 11 11 11 12 12 13 14 18 19; 14 19 18 19 19 19 10 10 11 11 10 10 10 11 11 11 11 11 11</pre>	
<pre>initial begin {monitor(\$time, " clk = %b, C = %b, Halt = %b", clk, C, Halt); clk = 0; in = 1; clk = 0; in = 1; cEz = 0; cEz = 0; define Resetz = 1; n = 0 = -127; // result expected : 3F01 #1 Resetz = 0; #1 Resetz = 1; wait(Halt); in = 0; f = 127; // result expected : C0FF #1 Resetz = 1; wait(Halt); in = 1; A = 127; // result expected : C0FF #1 Resetz = 1; wait(Halt); in = 1; A = 127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 1; wait(Halt); in = 1; A = 127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 1; wait(Halt); in = 1; A = 127; // result expected : C0FF</pre>	
<pre>\$monitor(\$time, " clk = %b, C = %b, Halt = %b", clk, C, Halt); clk = 0; im = 1; CEz = 0; Resetz = 1; A = -127; // result expected : 3F01 #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 1; wait(Halt); a im = 0; f = 127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 1; wait(Halt); im = 1; A = 127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 1; wait(Halt); f = -127; // result expected : C0FF #1 Resetz = 0; #1 Resetz = 0; #1 Resetz = 1; wait(Halt); f = -127; // result expected : C0FF #1 Resetz = 1; wait(Halt); #1 Resetz = 1; wait(Halt);</pre>	
<pre>12 13</pre>	
<pre>14 Im = 1; 15 CEz = 0; 16 Resetz = 1; 17 18 A = -127; 19 B = -127; // result expected : 3F01 20 #1 Resetz = 0; 21 #1 Resetz = 1; 22 wait(Halt); 23 24 Im = 0; 25 B = 127; // result expected : COFF 26 #1 Resetz = 0; 27 #1 Resetz = 1; 28 wait(Halt); 29 30 Im = 1; 31 A = 127; 32 B = -127; // result expected : COFF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 36</pre>	
<pre>15</pre>	
<pre>16</pre>	
<pre>17 18</pre>	
<pre>18</pre>	
<pre>19 B = -127; // result expected : 3F01 20 #1 Resetz = 0; 21 #1 Resetz = 1; 22 wait(Halt); 23 24 Im = 0; 25 B = 127; // result expected : C0FF 26 #1 Resetz = 0; 27 #1 Resetz = 1; 28 wait(Halt); 29 30 Im = 1; 31 A = 127; 32 B = -127; // result expected : C0FF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt); 36</pre>	
<pre>20 #1 Resetz = 0; 21 #1 Resetz = 1; 22 wait(Halt); 23 24 Im = 0; 25 B = 127; // result expected : COFF 26 #1 Resetz = 0; 27 #1 Resetz = 1; 28 wait(Halt); 29 30 Im = 1; 31 A = 127; 32 B = -127; // result expected : COFF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt);</pre>	
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<pre>23 24 Im = 0; 25 B = 127; // result expected : C0FF 26 #1 Resetz = 0; 27 #1 Resetz = 1; 28 wait(Halt); 29 30 Im = 1; 31 A = 127; 32 B = -127; // result expected : C0FF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt); 36</pre>	
<pre>24 Im = 0; 25 B = 127; // result expected : C0FF 26 #1 Resetz = 0; 27 #1 Resetz = 1; 28 wait(Halt); 29 30 Im = 1; 31 A = 127; 32 B = -127; // result expected : C0FF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt); 36</pre>	
<pre>25 B = 127; // result expected : C0FF 26 #1 Resetz = 0; 27 #1 Resetz = 1; 28 wait(Halt); 29 30 Im = 1; 31 A = 127; 32 B = -127; // result expected : C0FF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt); 36</pre>	
<pre>26 #1 Resetz = 0; 27 #1 Resetz = 1; 28 wait(Halt); 29 30 Im = 1; 31 A = 127; 32 B = -127; // result expected : COFF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt); 36</pre>	
<pre>27 #1 Resetz = 1; 28 wait(Halt); 29 30 Im = 1; 31 A = 127; 32 B = -127; // result expected : COFF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt); 36</pre>	
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29 30 Im = 1; 31 A = 127; 32 B = -127; // result expected : COFF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt); 36	
31 A = 127; 32 B = -127; // result expected : C0FF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt); 36	
32 B = -127; // result expected : COFF 33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt); 36	
33 #1 Resetz = 0; 34 #1 Resetz = 1; 35 wait(Halt); 36	
34 #1 Resetz = 1; 35 wait(Halt); 36	
35 wait(Halt); 36	
36	
38 B = 127; // result expected : 3F01	
39 #1 Resetz = 0;	
40 #1 Resetz = 1;	
41 wait(Halt);	
42	
43 #30 \$finish;	
44 end	
45	
46 always #5 clk = ~clk;	
47	-
endmodule	\leq

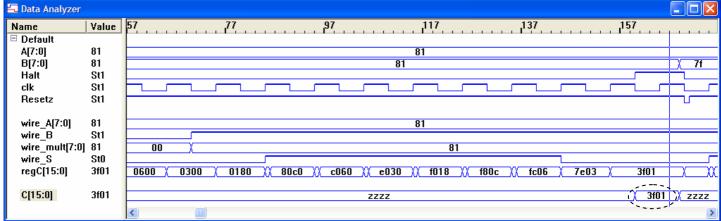
1	clk	=	Ο,	С	=	100000000000000,	Halt	=	0		
5	clk	=	1,	С	=	010000000000000,	Halt	=	0		
						1100000000000000,			0		
						1100000000000000,			0		
			-			011000000000000,			0		
						011000000000000,			0		
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			-			0000001100000000,			0		
			-			0000001100000000,					
			-			0000000110000000,					
80	clk	=	Ο,	С	=	000000110000000,	Halt	=	0		
85	clk	=	1,	С	=	000000011000000,	Halt	=	0		
86	clk	=	1,	С	=	100000011000000,	Halt	=	0		
90	clk	=	Ο,	С	=	100000011000000,	Halt	=	0		
95	clk	=	1,	C	=	010000001100000,	Halt	=	0		
96	clk	=	1,	С	=	110000001100000,	Halt	=	0		
			-			110000001100000,			0		
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			-			111000000110000,			õ		
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			-			111100000011000,					
			-			0111100000001100,			0		
						111110000001100,			0		
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						0111110000000110,		=	0		
136	clk	=	1,	С	=	111111000000110,	Halt	=	0		
140	clk	=	Ο,	С	=	111111000000110,	Halt	=	0		
145	clk	=	1,	С	=	011111100000011,	Halt	=	0		
150	clk	=	Ο,	С	=	0111111000000011,	Halt	=	0		
155	clk	=	1,	С	=	0011111100000001,	Halt	=	0		
160	clk	=	Ο,	С	=	0011111100000001,	Halt	=	1	=>	30F1
161	clk	=	ο,	С	=	1000000000000000,	Halt	=	0		
165	clk	=	1,	С	=	010000000000000,	Halt	=	0		
			-			1100000000000000,					
170	clk	=	Ο,								
				С	=	110000000000000,	Halt	=	0		
175	clk	=	1,	C C	=	110000000000000, 011000000000000,	Halt Halt	=	0 0		
175 176	clk clk	=	1, 1,	C C C	= = =	110000000000000, 011000000000000, 11100000000	Halt Halt Halt	= = =	0 0 0		
175 176 180	clk clk clk	= = =	1, 1, 0,	C C C C	= = =	110000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt	= = = =	0 0 0		
175 176 180 185	clk clk clk clk	= = =	1, 1, 0, 1,	C C C C C		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt	= = = =	0 0 0		
175 176 180 185 186	clk clk clk clk clk	= = =	1, 1, 0, 1, 1,	0 0 0 0 0 0 0		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt		0 0 0 0 0		
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175 176 180 185 186 190 195	clk clk clk clk clk clk clk		1, 1, 0, 1, 1, 0,	00000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt		0 0 0 0 0 0 0 0		
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175 176 180 185 186 190 195 196 200 205 206 210 215 216	clk clk clk clk clk clk clk clk clk clk		1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 1, 1,	00000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
175 176 180 185 186 190 195 196 200 205 206 210 215 216	clk clk clk clk clk clk clk clk clk clk		1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 1, 1,	00000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
175 176 180 185 186 190 195 196 200 205 206 210 215 216 220	clk clk clk clk clk clk clk clk clk clk		1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 1, 0, 1, 0,	0000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		$\begin{smallmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 $		
175 176 180 185 186 190 195 196 200 205 206 210 215 216 220 225	clk clk clk clk clk clk clk clk clk clk		1,,0,1,0,1,1,0,1,1,0,1,1,0,1,	0000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 195 196 200 205 206 210 215 216 220 225 226	clk clk clk clk clk clk clk clk clk clk		1,,0,1,1,0,1,1,0,1,1,0,1,1,0,1,1,0,1,1,0,1,1,0,1,1,0,1,1,0,1,1,0,1,1,0,1,1,0,1,1,0,1,1,1,0,1,000000	000000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 195 200 205 206 210 215 216 220 225 226 230	clk clk clk clk clk clk clk clk clk clk		1,,0,1,0,1,0,1,0,1,0,1,1,0,1,1,0,	000000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 195 200 205 206 210 215 216 220 225 226 230 235	clk clk clk clk clk clk clk clk clk clk		1,,0,1,0,1,0,1,0,1,0,1,0,1,0,1,0,1,0,1,	00000000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 195 196 200 205 206 210 215 216 220 225 226 230 235 236	clk clk clk clk clk clk clk clk clk clk		1,,0,1,0,1,0,1,0,1,0,1,0,11,1,0,11,1,0,11,1,0,11,10,11,10,11,10,11,10,11,10,11,10,11,10,11,10,11,10,11,10,11,10,11,10,11,10,11,10,11,10,111,10,111,10,111,10,111,10,111,10,111,10,111111	000000000000000000000000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 195 196 200 205 206 210 215 216 220 225 226 230 235 236 240	clk clk clk clk clk clk clk clk clk clk		1,,01,01,01,01,01,0,1,0,1,0,0,00,00,00,0	000000000000000000000000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 215 216 220 225 226 230 235 236 240 245	clk clk clk clk clk clk clk clk clk clk		1,,01,,01,01,01,01,0,01,001,000,00000000	000000000000000000000000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 215 216 220 225 226 230 235 236 240 245 250	clk clk clk clk clk clk clk clk clk clk		1,,01,01,01101,01,0,01,0,01,0,01,0,000,0000,0000,0000,0000,0000,0000,0000	000000000000000000000000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 225 226 230 225 226 230 235 236 240 245 250 255	clk clk clk clk clk clk clk clk clk clk		1,,01,01,01,01,01,01,01,01,01,01,01,01,0	000000000000000000000000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 225 226 230 235 236 240 245 250 255 260	clk clk clk clk clk clk clk clk clk clk		1,,,,1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	000000000000000000000000000000000000000		1100000000000000, 011000000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 215 226 230 235 236 240 245 255 260 265	clk clk clk clk clk clk clk clk clk clk		1,,,,1,,,1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	000000000000000000000000000000000000000		1100000000000000, 01100000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 195 200 205 206 210 215 226 230 235 236 240 245 255 255 260 255 260 265 270	clk clk clk clk clk clk clk clk clk clk		1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	000000000000000000000000000000000000000		1100000000000000, 01100000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 215 216 220 225 226 230 235 236 240 245 255 260 255 260 270 275	clk clk clk clk clk clk clk clk clk clk		1,,,1,0,1,0,1,0,1,0,1,0,1,0,1,0,1,0,1,0	000000000000000000000000000000000000000		<pre>1100000000000000, 011000000000000, 11100000000</pre>	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 215 216 220 235 226 230 235 236 240 245 250 255 260 245 250 265 270 275 280	clk clk clk clk clk clk clk clk clk clk		1,,,1,0,1,0,1,0,1,0,1,0,1,0,1,0,1,0,1,0	000000000000000000000000000000000000000		1100000000000000, 01100000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 225 226 230 225 226 230 235 226 230 245 255 260 245 255 260 265 275 280 285	clk clk clk clk clk clk clk clk clk clk		1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	000000000000000000000000000000000000000		110000000000000, 01100000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 225 226 230 235 226 230 235 226 230 245 255 260 245 255 260 245 255 260 245 255 260 245 275 280 285 290	clk clk clk clk clk clk clk clk clk clk		1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	000000000000000000000000000000000000000		110000000000000, 01100000000000, 11100000000	Halt Halt Halt Halt Halt Halt Halt Halt		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
175 176 180 185 186 190 205 206 210 225 226 230 235 226 230 235 236 240 245 255 260 265 270 265 270 265 270 285 280 295	clk		1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,			<pre>1100000000000000, 011000000000000, 11100000000</pre>	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 225 226 230 235 236 240 245 255 260 255 260 255 260 255 260 255 270 275 285 290 295 300	clk		1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	000000000000000000000000000000000000000		<pre>1100000000000000, 011000000000000, 11100000000</pre>	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 215 226 230 235 226 230 245 255 260 255 250 255 260 255 255	clk		110110110110110110110101010101010101	000000000000000000000000000000000000000		<pre>1100000000000000, 011000000000000, 11100000000</pre>	Halt Halt Halt Halt Halt Halt Halt Halt		000000000000000000000000000000000000000		
175 176 180 185 186 190 205 206 210 215 226 230 235 236 240 245 255 260 255 260 255 260 265 270 265 270 265 270 265 270 265 270 275 280 295 300 305 306	clk		110110110110110110110101010101010101011	000000000000000000000000000000000000000		<pre>1100000000000000, 011000000000000, 11100000000</pre>	Halt Halt Halt Halt Halt Halt Halt Halt		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
175 176 180 185 186 190 205 206 210 215 226 230 235 236 240 245 255 260 255 260 255 260 265 270 265 270 265 270 265 270 265 270 275 280 295 300 305 306	clk		110110110110110110110101010101010101011	000000000000000000000000000000000000000		<pre>1100000000000000, 011000000000000, 11100000000</pre>	Halt Halt Halt Halt Halt Halt Halt Halt		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
175 176 180 185 186 190 205 206 210 215 216 220 225 226 230 235 236 240 245 250 265 270 275 280 275 280 275 280 275 280 275 280 275 290 305 306 310	clk		1101101101101101101101010101010101010101	000000000000000000000000000000000000000		<pre>1100000000000000, 011000000000000, 11100000000</pre>	Halt Halt Halt Halt Halt Halt Halt Halt				
175 176 180 185 186 190 205 206 210 215 216 220 235 226 230 235 226 230 245 255 260 245 255 260 245 255 260 275 280 285 290 305 306 310 315	clk		1101101101101101101101010101010101010101	000000000000000000000000000000000000000		<pre>1100000000000000, 011000000000000, 11100000000</pre>	Halt Halt Halt Halt Halt Halt Halt Halt				
175 176 180 185 186 190 195 206 210 205 206 210 225 226 230 235 226 230 245 250 255 260 245 255 260 245 255 260 245 255 260 245 255 260 245 255 260 245 255 260 245 255 260 245 255 260 245 255 260 245 255 260 245 255 260 245 255 260 245 255 260 245 255 260 275 260 255 260 265 275 260 275 275 260 275 275 260 275 275 260 275 275 260 275 275 260 275 275 260 275 275 260 275 275 276 275 275 276 275 275 275 275 275 275 275 275 275 275	clk		1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	000000000000000000000000000000000000000		<pre>1100000000000000, 011000000000000, 11100000000</pre>	Halt Halt Halt Halt Halt Halt Halt Halt		$\begin{smallmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 &$	=>	C0FF

321 clk = 0, C =	1000000000000000,	Halt = 0	
325 clk = 1, C =	0100000000000000,	Halt = 0	
-	1100000000000000,		
	1100000000000000,		
	0110000000000000,		
	1110000000000000000,		
•	11100000000000000000,		
	011100000000000,		
	1111000000000000,		
	1111000000000000,		
	0111100000000000,		
	1111100000000000,		
$360 \ clk = 0, C =$	111110000000000,	Halt = 0	
365 clk = 1, C =	011111000000000,	Halt = 0	
366 clk = 1, C =	111111000000000,	Halt = 0	
$370 \ clk = 0, C =$	111111000000000,	Halt = 0	
375 clk = 1, C =	0111111000000000,	Halt = 0	
-	1111111000000000,		
	111111100000000,		
	0111111100000000,		
	1111111100000000,		
	1111111100000000,		
-	0111111110000000,		
-	111111110000000,		
-	111111110000000,		
-	0111111111000000,		
-	011111111000000,		
	001111111100000,		
420 clk = 0, C =	001111111100000,	Halt = 0	
425 clk = 1, C =	0001111111110000,	Halt = 0	
$430 \ clk = 0, C =$	0001111111110000,	Halt = 0	
435 clk = 1, C =	0000111111111000,	Halt = 0	
-	0000111111111000,		
	0000011111111100,		
	0000011111111100,		
	000000111111110,		
	000000111111110,		
-	-		
-	000000111111111,		
-	100000111111111,		
	1000000111111111,		
475 clk = 1, C =	0100000011111111,	TT = 1 + - 0	
	1100000011111111,		
476 clk = 1, C = 480 clk = 0, C =	1100000011111111, <u>1100000011111111</u> ,	Halt = 0 Halt = 1	=> COFF
476 clk = 1, C = 480 clk = 0, C =	1100000011111111,	Halt = 0 Halt = 1	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C =	1100000011111111, <u>1100000011111111</u> ,	$\begin{array}{l} \text{Halt} = 0\\ \text{Halt} = 1\\ \text{Halt} = 0 \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C =	110000011111111, <u>1100000011111111</u> , 100000000000000, 010000000000	Halt = 0 $Halt = 1$ $Halt = 0$ $Halt = 0$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C =	110000011111111, <u>1100000011111111</u> , 100000000000000, 010000000000	$\begin{array}{rrrr} \text{Halt} &=& 0\\ \text{Halt} &=& 1\\ \text{Halt} &=& 0\\ \text{Halt} &=& 0\\ \text{Halt} &=& 0 \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C =	110000011111111, <u>1100000011111111</u> , 100000000000000, 010000000000	$\begin{array}{rrrr} \text{Halt} &=& 0\\ \text{Halt} &=& 1\\ \text{Halt} &=& 0\\ \text{Halt} &=& 0\\ \text{Halt} &=& 0\\ \text{Halt} &=& 0 \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C =	110000011111111, <u>1100000011111111</u> , 100000000000000, 010000000000000, 110000000000	$ Halt = 0 \\ Halt = 1 \\ Halt = 0 $	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 500 clk = 0, C =	110000011111111, <u>1100000011111111</u> , 1000000000000000, 010000000000000, 110000000000	Halt = 0 Halt = 1 Halt = 0 Halt = 0 Halt = 0 Halt = 0 Halt = 0 Halt = 0	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 1, C =	110000011111111, <u>1100000011111111,</u> 100000000000000, 01000000000000, 110000000000	$ Halt = 0 \\ Halt = 1 \\ Halt = 0 \\ Halt $	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 500 clk = 1, C = 505 clk = 1, C = 510 clk = 0, C =	110000011111111, <u>110000011111111</u> , 100000000000000, 01000000000000, 110000000000	$ Halt = 0 \\ Halt = 1 \\ Halt = 0 \\ Halt $	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 510 clk = 0, C = 515 clk = 1, C =	110000011111111, <u>1100000011111111,</u> 100000000000000, 01000000000000, 110000000000	$ Halt = 0 \\ Halt = 1 \\ Halt = 0 \\ Halt $	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C =	110000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000000, 110000000000	$ Halt = 0 \\ Halt = 1 \\ Halt = 0 \\ Halt $	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 510 clk = 1, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C =	110000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000000, 110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 530 clk = 0, C =	110000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000000, 110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 515 clk = 1, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 530 clk = 0, C = 535 clk = 1,	110000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000000, 110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 530 clk = 0, C = 535 clk = 1, C = 540 clk = 0, C = 540 clk = 0, C =	110000011111111, <u>1100000011111111,</u> 100000000000000, 01000000000000, 110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 500 clk = 0, C = 505 clk = 1, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 530 clk = 0, C = 535 clk = 1, C = 540 clk = 0, C = 545 clk = 1,	110000011111111, <u>110000011111111</u> , 1000000000000000, 010000000000000, 110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 505 clk = 1, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 535 clk = 1, C = 535 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 550 clk = 0,	1100000011111111, <u>1100000011111111</u> , 1000000000000000, 010000000000000, 110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 505 clk = 1, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 1, C = 540 clk = 1, C = 541 clk = 1, C = 542 clk = 1, C = 543 clk = 1, C = 544 clk = 1, C = 545 clk = 1,	<pre>1100000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000</pre>	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 530 clk = 0, C = 535 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 555 clk = 1, C = 560 clk = 0,	<pre>1100000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000</pre>	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 530 clk = 0, C = 535 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 555 clk = 1, C = 560 clk = 0,	<pre>1100000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000</pre>	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 485 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 505 clk = 1, C = 505 clk = 1, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 535 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 555 clk = 1, C = 560 clk = 0, C = 565 clk = 1, C = 566 clk = 1, C = 566 clk = 1, C = 561 clk = 1, C = 566 clk = 1, C = 561 clk = 1, C = 566 clk = 1, C = 561 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1,	1100000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000000, 110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 485 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 505 clk = 1, C = 505 clk = 1, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 535 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 555 clk = 1, C = 560 clk = 0, C = 565 clk = 1, C = 566 clk = 1, C = 566 clk = 1, C = 561 clk = 1, C = 566 clk = 1, C = 561 clk = 1, C = 566 clk = 1, C = 561 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1, C = 566 clk = 1, C = 565 clk = 1,	1100000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000000, 110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 485 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 505 clk = 1, C = 505 clk = 1, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 535 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 555 clk = 1, C = 560 clk = 1, C = 566 clk = 1, C = 570 clk = 0,	1100000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000000, 110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \ \ \text{Halt} &= & 0 \\ \ \ \text{Halt} &= & 0 \\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 505 clk = 1, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 530 clk = 0, C = 535 clk = 1, C = 540 clk = 0, C = 540 clk = 0, C = 545 clk = 1, C = 550 clk = 1, C = 555 clk = 1, C = 566 clk = 1, C = 575 clk = 1, C =	<pre>1100000011111111, 1100000011111111, 100000000</pre>	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
$\begin{array}{rcl} 476 & clk = 1, \ C = \\ 480 & clk = 0, \ C = \\ 481 & clk = 0, \ C = \\ 485 & clk = 1, \ C = \\ 486 & clk = 1, \ C = \\ 490 & clk = 0, \ C = \\ 495 & clk = 1, \ C = \\ 500 & clk = 0, \ C = \\ 500 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 520 & clk = 1, \ C = \\ 520 & clk = 1, \ C = \\ 520 & clk = 1, \ C = \\ 530 & clk = 0, \ C = \\ 535 & clk = 1, \ C = \\ 535 & clk = 1, \ C = \\ 540 & clk = 0, \ C = \\ 540 & clk = 0, \ C = \\ 555 & clk = 1, \ C = \\ 550 & clk = 0, \ C = \\ 555 & clk = 1, \ C = \\ 566 & clk = 1, \ C = \\ 576 & clk = 1$	<pre>1100000011111111, <u>1100000011111111,</u> 1000000000000000, 010000000000</pre>	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 505 clk = 1, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 530 clk = 0, C = 535 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 555 clk = 1, C = 560 clk = 1, C = 566 clk = 1, C = 570 clk = 1, C = 576 clk = 1, C = 580 clk = 1, C = 580 clk = 1, C = 576 clk = 1, C = 580 clk = 0, C = 580 clk = 0, C = 580 clk = 1, C = 580 clk = 0, C = 580 clk = 1, C = 580 clk = 0,	1100000011111111, <u>1100000011111111</u> , 1000000000000000, 010000000000000, 110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
$\begin{array}{rcl} 476 & clk = 1, \ C = \\ 480 & clk = 0, \ C = \\ 481 & clk = 0, \ C = \\ 485 & clk = 1, \ C = \\ 486 & clk = 1, \ C = \\ 490 & clk = 0, \ C = \\ 495 & clk = 1, \ C = \\ 500 & clk = 0, \ C = \\ 505 & clk = 1, \ C = \\ 510 & clk = 0, \ C = \\ 515 & clk = 1, \ C = \\ 520 & clk = 0, \ C = \\ 525 & clk = 1, \ C = \\ 520 & clk = 0, \ C = \\ 535 & clk = 1, \ C = \\ 540 & clk = 0, \ C = \\ 545 & clk = 1, \ C = \\ 550 & clk = 1, \ C = \\ 545 & clk = 1, \ C = \\ 550 & clk = 1, \ C = \\ 560 & clk = 0, \ C = \\ 566 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 580 & clk = 0, \ C = \\ 585 & clk = 1$	<pre>1100000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000</pre>	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
476 clk = 1, C = 480 clk = 0, C = 481 clk = 0, C = 485 clk = 1, C = 486 clk = 1, C = 490 clk = 0, C = 495 clk = 1, C = 500 clk = 0, C = 510 clk = 0, C = 515 clk = 1, C = 520 clk = 0, C = 525 clk = 1, C = 530 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 545 clk = 1, C = 540 clk = 0, C = 555 clk = 1, C = 560 clk = 0, C = 565 clk = 1, C = 566 clk = 1, C = 576 clk = 1, C = 576 clk = 1, C = 580 clk = 0, C = 585 clk = 1, C = 576 clk = 1, C = 580 clk = 1, C = 585 clk = 1, C = 586 clk = 1,	<pre>1100000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000</pre>	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \end{array}$	=> COFF
$\begin{array}{rcl} 476 & clk = 1, \ C = \\ 480 & clk = 0, \ C = \\ 481 & clk = 0, \ C = \\ 485 & clk = 1, \ C = \\ 486 & clk = 1, \ C = \\ 490 & clk = 0, \ C = \\ 495 & clk = 1, \ C = \\ 500 & clk = 0, \ C = \\ 505 & clk = 1, \ C = \\ 510 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 520 & clk = 1, \ C = \\ 520 & clk = 1, \ C = \\ 520 & clk = 1, \ C = \\ 530 & clk = 0, \ C = \\ 535 & clk = 1, \ C = \\ 530 & clk = 0, \ C = \\ 545 & clk = 1, \ C = \\ 545 & clk = 1, \ C = \\ 550 & clk = 0, \ C = \\ 555 & clk = 1, \ C = \\ 560 & clk = 0, \ C = \\ 565 & clk = 1, \ C = \\ 566 & clk = 1, \ C = \\ 570 & clk = 0, \ C = \\ 576 & clk = 1, \ C = \\ 580 & clk = 1, \ C = \\ 580 & clk = 1, \ C = \\ 586 & clk = 1, \ C = \\ 586 & clk = 1, \ C = \\ 590 & clk = 0, \ C = \\ \end{array}$	1100000011111111, <u>1100000011111111</u> , <u>10000000000000000</u> , 010000000000000, 110000000000000, 0110000000000	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \text{Halt} &= & 1 \\ \text{Halt} &= & 0 \\ \ \text{Halt} &= & 0 \\ \text{Halt} &= & 0 \\ \ \ \text{Halt} &= & 0 \\ \ \ \text{Halt} &= & 0 \\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	=> COFF
$\begin{array}{rcl} 476 & clk = 1, \ C = \\ 480 & clk = 0, \ C = \\ 481 & clk = 0, \ C = \\ 485 & clk = 1, \ C = \\ 486 & clk = 1, \ C = \\ 490 & clk = 0, \ C = \\ 495 & clk = 1, \ C = \\ 500 & clk = 0, \ C = \\ 505 & clk = 1, \ C = \\ 510 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 520 & clk = 1, \ C = \\ 520 & clk = 1, \ C = \\ 520 & clk = 1, \ C = \\ 530 & clk = 0, \ C = \\ 535 & clk = 1, \ C = \\ 530 & clk = 0, \ C = \\ 540 & clk = 0, \ C = \\ 540 & clk = 0, \ C = \\ 555 & clk = 1, \ C = \\ 550 & clk = 0, \ C = \\ 555 & clk = 1, \ C = \\ 560 & clk = 0, \ C = \\ 566 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 586 & clk = 1, \ C = \\ 585 & clk = 1, \ C = \\ 586 & clk = 1, \ C = \\ 586 & clk = 1, \ C = \\ 586 & clk = 1, \ C = \\ 590 & clk = 0, \ C = \\ 590 & clk = 0, \ C = \\ 590 & clk = 1, \ C = \\ 50 & clk = 1, \ C = \\ 50 & clk = 1, \ C = \\ 50 & clk = 1, \ C = \\ 50 & clk = 1, \ C = \\ 50 & clk = 1, \ C = \\ 50 & clk = 1, \ C = \\ 50 & clk = 1, \ C = \\ 50 & clk = 1, \ C = \\ 50 & clk = 1, \ C = \\ 50 & clk = 1, \ C = \\ $	<pre>1100000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000</pre>	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \ \ \text{Halt} &= & 0 \\ \ \ \text{Halt} &= & 0 \\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	=> COFF
$\begin{array}{rcl} 476 & clk = 1, \ C = \\ 480 & clk = 0, \ C = \\ 481 & clk = 0, \ C = \\ 485 & clk = 1, \ C = \\ 486 & clk = 1, \ C = \\ 490 & clk = 0, \ C = \\ 495 & clk = 1, \ C = \\ 500 & clk = 0, \ C = \\ 505 & clk = 1, \ C = \\ 510 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 520 & clk = 1, \ C = \\ 520 & clk = 0, \ C = \\ 520 & clk = 0, \ C = \\ 520 & clk = 0, \ C = \\ 535 & clk = 1, \ C = \\ 530 & clk = 0, \ C = \\ 540 & clk = 0, \ C = \\ 540 & clk = 0, \ C = \\ 540 & clk = 0, \ C = \\ 555 & clk = 1, \ C = \\ 550 & clk = 1, \ C = \\ 560 & clk = 0, \ C = \\ 565 & clk = 1, \ C = \\ 566 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 580 & clk = 0, \ C = \\ 585 & clk = 1, \ C = \\ 580 & clk = 0, \ C = \\ 586 & clk = 1, \ C = \\ 590 & clk = 0, \ C = \\ 595 & clk = 1, \ C = \\ 596 & clk = 1$	<pre>1100000011111111, 1100000011111111, 100000000</pre>	Halt = 0 Halt = 1 Halt = 0 Halt = 0	=> COFF
$\begin{array}{rcl} 476 & clk = 1, \ C = \\ 480 & clk = 0, \ C = \\ 481 & clk = 0, \ C = \\ 485 & clk = 1, \ C = \\ 486 & clk = 1, \ C = \\ 490 & clk = 0, \ C = \\ 495 & clk = 1, \ C = \\ 500 & clk = 0, \ C = \\ 505 & clk = 1, \ C = \\ 510 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 510 & clk = 0, \ C = \\ 520 & clk = 1, \ C = \\ 520 & clk = 1, \ C = \\ 520 & clk = 1, \ C = \\ 535 & clk = 1, \ C = \\ 535 & clk = 1, \ C = \\ 535 & clk = 1, \ C = \\ 540 & clk = 0, \ C = \\ 540 & clk = 0, \ C = \\ 555 & clk = 1, \ C = \\ 550 & clk = 1, \ C = \\ 560 & clk = 0, \ C = \\ 566 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 580 & clk = 1, \ C = \\ 586 & clk = 1, \ C = \\ 586 & clk = 1, \ C = \\ 596 & clk = 0, \ C = \\ 596 & clk = 0$	<pre>1100000011111111, <u>1100000011111111,</u> 1000000000000000, 010000000000</pre>	Halt = 0 Halt = 1 Halt = 0 Halt = 0	=> COFF
$\begin{array}{rcl} 476 & \text{clk} = 1, & \text{C} = \\ 480 & \text{clk} = 0, & \text{C} = \\ 481 & \text{clk} = 0, & \text{C} = \\ 485 & \text{clk} = 1, & \text{C} = \\ 486 & \text{clk} = 1, & \text{C} = \\ 490 & \text{clk} = 0, & \text{C} = \\ 495 & \text{clk} = 1, & \text{C} = \\ 500 & \text{clk} = 0, & \text{C} = \\ 500 & \text{clk} = 0, & \text{C} = \\ 510 & \text{clk} = 1, & \text{C} = \\ 510 & \text{clk} = 1, & \text{C} = \\ 510 & \text{clk} = 1, & \text{C} = \\ 520 & \text{clk} = 1, & \text{C} = \\ 520 & \text{clk} = 1, & \text{C} = \\ 520 & \text{clk} = 1, & \text{C} = \\ 535 & \text{clk} = 1, & \text{C} = \\ 535 & \text{clk} = 1, & \text{C} = \\ 540 & \text{clk} = 0, & \text{C} = \\ 540 & \text{clk} = 0, & \text{C} = \\ 540 & \text{clk} = 1, & \text{C} = \\ 550 & \text{clk} = 1, & \text{C} = \\ 550 & \text{clk} = 1, & \text{C} = \\ 560 & \text{clk} = 1, & \text{C} = \\ 566 & \text{clk} = 1, & \text{C} = \\ 576 & \text{clk} = 1, & \text{C} = \\ 580 & \text{clk} = 1, & \text{C} = \\ 580 & \text{clk} = 1, & \text{C} = \\ 586 & \text{clk} = 1, & \text{C} = \\ 596 & \text$	<pre>1100000011111111, <u>1100000011111111,</u> 1000000000000000, 010000000000</pre>	Halt = 0 Halt = 1 Halt = 0 Halt = 0	=> COFF
$\begin{array}{rcl} 476 & clk = 1, \ C = \\ 480 & clk = 0, \ C = \\ 481 & clk = 0, \ C = \\ 485 & clk = 1, \ C = \\ 486 & clk = 1, \ C = \\ 490 & clk = 0, \ C = \\ 495 & clk = 1, \ C = \\ 500 & clk = 0, \ C = \\ 505 & clk = 1, \ C = \\ 510 & clk = 0, \ C = \\ 515 & clk = 1, \ C = \\ 520 & clk = 0, \ C = \\ 525 & clk = 1, \ C = \\ 530 & clk = 0, \ C = \\ 535 & clk = 1, \ C = \\ 530 & clk = 0, \ C = \\ 535 & clk = 1, \ C = \\ 540 & clk = 0, \ C = \\ 555 & clk = 1, \ C = \\ 550 & clk = 1, \ C = \\ 560 & clk = 0, \ C = \\ 565 & clk = 1, \ C = \\ 566 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 576 & clk = 1, \ C = \\ 580 & clk = 0, \ C = \\ 585 & clk = 1, \ C = \\ 586 & clk = 1, \ C = \\ 590 & clk = 0, \ C = \\ 595 & clk = 1, \ C = \\ 596 & clk = 1, \ C = \\ 596 & clk = 1, \ C = \\ 596 & clk = 1, \ C = \\ 600 & clk = 0, \ C = \\ 605 & clk = 1, \ C = \\ 606 & clk = 1, \ C = \\ 606 & clk = 1, \ C = \\ \end{array}$	<pre>1100000011111111, <u>1100000011111111,</u> 100000000000000, 010000000000</pre>	$\begin{array}{rrrr} \text{Halt} &= & 0 \\ \ \ \text{Halt} &= & 0 \\ \ \ \text{Halt} &= & 0 \\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	=> COFF
$\begin{array}{l} 476 \ clk = 1, \ C = \\ 480 \ clk = 0, \ C = \\ 481 \ clk = 0, \ C = \\ 485 \ clk = 1, \ C = \\ 486 \ clk = 1, \ C = \\ 490 \ clk = 0, \ C = \\ 495 \ clk = 1, \ C = \\ 500 \ clk = 0, \ C = \\ 505 \ clk = 1, \ C = \\ 510 \ clk = 0, \ C = \\ 515 \ clk = 1, \ C = \\ 520 \ clk = 0, \ C = \\ 525 \ clk = 1, \ C = \\ 520 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 530 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 540 \ clk = 0, \ C = \\ 540 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 560 \ clk = 0, \ C = \\ 565 \ clk = 1, \ C = \\ 566 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 580 \ clk = 0, \ C = \\ 585 \ clk = 1, \ C = \\ 586 \ clk = 1, \ C = \\ 590 \ clk = 0, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 610 \ clk = 0, $	<pre>1100000011111111, 1000000000000000, 0100000000</pre>	$\begin{array}{rcl} \text{Halt} &= & 0 \\ \ \ \text{Halt} &= & 0 \\ \ \ \text{Halt} &= & 0 \\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	=> COFF
$\begin{array}{l} 476 \ clk = 1, \ C = \\ 480 \ clk = 0, \ C = \\ 481 \ clk = 0, \ C = \\ 485 \ clk = 1, \ C = \\ 486 \ clk = 1, \ C = \\ 490 \ clk = 0, \ C = \\ 495 \ clk = 1, \ C = \\ 500 \ clk = 0, \ C = \\ 505 \ clk = 1, \ C = \\ 510 \ clk = 0, \ C = \\ 510 \ clk = 0, \ C = \\ 510 \ clk = 0, \ C = \\ 520 \ clk = 1, \ C = \\ 520 \ clk = 0, \ C = \\ 520 \ clk = 0, \ C = \\ 530 \ clk = 0, \ C = \\ 530 \ clk = 0, \ C = \\ 530 \ clk = 0, \ C = \\ 545 \ clk = 1, \ C = \\ 540 \ clk = 0, \ C = \\ 545 \ clk = 1, \ C = \\ 540 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 560 \ clk = 0, \ C = \\ 565 \ clk = 1, \ C = \\ 566 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 580 \ clk = 1, \ C = \\ 580 \ clk = 1, \ C = \\ 590 \ clk = 0, \ C = \\ 595 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 600 \ clk = 0, \ C = \\ 605 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 610 \ clk = 0, \ C = \\ 615 \ clk = 1, \ C = \\ 615 \ clk = 1, \ C = \\ 616 \ clk = 1, \ C = \\ 615 \ clk = 1, \ C = \\ 616 \ clk = 1, $	<pre>1100000011111111, 11000000000000000, 0100000000</pre>	Halt = 0 Halt = 1 Halt = 0 Halt = 0	=> COFF
$\begin{array}{l} 476 \ clk = 1, \ C = \\ 480 \ clk = 0, \ C = \\ 481 \ clk = 0, \ C = \\ 485 \ clk = 1, \ C = \\ 486 \ clk = 1, \ C = \\ 490 \ clk = 0, \ C = \\ 495 \ clk = 1, \ C = \\ 500 \ clk = 0, \ C = \\ 505 \ clk = 1, \ C = \\ 510 \ clk = 0, \ C = \\ 515 \ clk = 1, \ C = \\ 520 \ clk = 0, \ C = \\ 525 \ clk = 1, \ C = \\ 520 \ clk = 0, \ C = \\ 525 \ clk = 1, \ C = \\ 530 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 540 \ clk = 0, \ C = \\ 545 \ clk = 1, \ C = \\ 540 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 560 \ clk = 0, \ C = \\ 565 \ clk = 1, \ C = \\ 566 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 580 \ clk = 1, \ C = \\ 580 \ clk = 1, \ C = \\ 590 \ clk = 0, \ C = \\ 595 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 600 \ clk = 0, \ C = \\ 605 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 610 \ clk = 0, \ C = \\ 615 \ clk = 1, \ C = \\ 616 \ clk = 1, $	<pre>1100000011111111, 11000000000000000, 0100000000</pre>	Halt = 0 Halt = 1 Halt = 0 Halt = 0	=> COFF
$\begin{array}{c} 476 \ clk = 1, \ C = \\ 480 \ clk = 0, \ C = \\ 481 \ clk = 0, \ C = \\ 485 \ clk = 1, \ C = \\ 486 \ clk = 1, \ C = \\ 490 \ clk = 0, \ C = \\ 495 \ clk = 1, \ C = \\ 500 \ clk = 0, \ C = \\ 505 \ clk = 1, \ C = \\ 510 \ clk = 0, \ C = \\ 515 \ clk = 1, \ C = \\ 520 \ clk = 0, \ C = \\ 520 \ clk = 0, \ C = \\ 520 \ clk = 0, \ C = \\ 520 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 530 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 540 \ clk = 0, \ C = \\ 540 \ clk = 0, \ C = \\ 545 \ clk = 1, \ C = \\ 550 \ clk = 1, \ C = \\ 550 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 566 \ clk = 1, \ C = \\ 566 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 580 \ clk = 0, \ C = \\ 585 \ clk = 1, \ C = \\ 586 \ clk = 1, \ C = \\ 590 \ clk = 0, \ C = \\ 595 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 600 \ clk = 0, \ C = \\ 605 \ clk = 1, \ C = \\ 600 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 616 \ clk = 1, \ C = \\ 616 \ clk = 1, \ C = \\ 616 \ clk = 1, \ C = \\ 620 \ clk = 0, $	<pre>1100000011111111, 1100000011111111, 100000000</pre>	Halt = 0 Halt = 1 Halt = 0 Halt = 0	=> COFF
$\begin{array}{c} 476 \ clk = 1, \ C = \\ 480 \ clk = 0, \ C = \\ 481 \ clk = 0, \ C = \\ 485 \ clk = 1, \ C = \\ 486 \ clk = 1, \ C = \\ 490 \ clk = 0, \ C = \\ 495 \ clk = 1, \ C = \\ 500 \ clk = 0, \ C = \\ 505 \ clk = 1, \ C = \\ 510 \ clk = 0, \ C = \\ 510 \ clk = 0, \ C = \\ 510 \ clk = 0, \ C = \\ 520 \ clk = 1, \ C = \\ 520 \ clk = 1, \ C = \\ 520 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 530 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 540 \ clk = 0, \ C = \\ 540 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 550 \ clk = 1, \ C = \\ 560 \ clk = 0, \ C = \\ 565 \ clk = 1, \ C = \\ 566 \ clk = 1, \ C = \\ 566 \ clk = 1, \ C = \\ 570 \ clk = 0, \ C = \\ 576 \ clk = 1, \ C = \\ 580 \ clk = 1, \ C = \\ 580 \ clk = 1, \ C = \\ 586 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 600 \ clk = 0, \ C = \\ 605 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 610 \ clk = 0, \ C = \\ 615 \ clk = 1, \ C = \\ 620 \ clk = 0, \ C = \\ 625 \ clk = 1, \ C = \\ 620 \ clk = 0, \ C = \\ 625 \ clk = 1, \ C = \\ 620 \ clk = 0, \ C = \\ 625 \ clk = 1, $	<pre>1100000011111111, 1100000011111111, 100000000</pre>	Halt = 0 Halt = 1 Halt = 0 Halt = 0	=> COFF
$\begin{array}{c} 476 \ clk = 1, \ C = \\ 480 \ clk = 0, \ C = \\ 481 \ clk = 0, \ C = \\ 485 \ clk = 1, \ C = \\ 486 \ clk = 1, \ C = \\ 490 \ clk = 0, \ C = \\ 495 \ clk = 1, \ C = \\ 500 \ clk = 0, \ C = \\ 505 \ clk = 1, \ C = \\ 510 \ clk = 0, \ C = \\ 510 \ clk = 0, \ C = \\ 510 \ clk = 0, \ C = \\ 520 \ clk = 1, \ C = \\ 520 \ clk = 1, \ C = \\ 520 \ clk = 1, \ C = \\ 530 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 530 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 540 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 550 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 560 \ clk = 0, \ C = \\ 566 \ clk = 1, \ C = \\ 566 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 586 \ clk = 1, \ C = \\ 586 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 600 \ clk = 0, \ C = \\ 605 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 610 \ clk = 0, \ C = \\ 615 \ clk = 1, \ C = \\ 616 \ clk = 1, \ C = \\ 620 \ clk = 0, \ C = \\ 625 \ clk = 1, \ C = \\ 630 \ clk = 0, $	<pre>1100000011111111, 11000000000000000, 0100000000</pre>	Halt = 0 Halt = 1 Halt = 0 Halt = 0	
$\begin{array}{c} 476 \ clk = 1, \ C = \\ 480 \ clk = 0, \ C = \\ 481 \ clk = 0, \ C = \\ 485 \ clk = 1, \ C = \\ 486 \ clk = 1, \ C = \\ 490 \ clk = 0, \ C = \\ 495 \ clk = 1, \ C = \\ 500 \ clk = 0, \ C = \\ 505 \ clk = 1, \ C = \\ 510 \ clk = 0, \ C = \\ 510 \ clk = 0, \ C = \\ 510 \ clk = 0, \ C = \\ 520 \ clk = 1, \ C = \\ 520 \ clk = 1, \ C = \\ 520 \ clk = 1, \ C = \\ 530 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 530 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 540 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 550 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 560 \ clk = 0, \ C = \\ 566 \ clk = 1, \ C = \\ 566 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 586 \ clk = 1, \ C = \\ 586 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 600 \ clk = 0, \ C = \\ 605 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 610 \ clk = 0, \ C = \\ 615 \ clk = 1, \ C = \\ 616 \ clk = 1, \ C = \\ 620 \ clk = 0, \ C = \\ 625 \ clk = 1, \ C = \\ 630 \ clk = 0, $	<pre>1100000011111111, 1100000011111111, 100000000</pre>	Halt = 0 Halt = 1 Halt = 0 Halt = 0	
$\begin{array}{c} 476 \ clk = 1, \ C = \\ 480 \ clk = 0, \ C = \\ 481 \ clk = 0, \ C = \\ 485 \ clk = 1, \ C = \\ 486 \ clk = 1, \ C = \\ 490 \ clk = 0, \ C = \\ 495 \ clk = 1, \ C = \\ 500 \ clk = 0, \ C = \\ 505 \ clk = 1, \ C = \\ 510 \ clk = 0, \ C = \\ 510 \ clk = 0, \ C = \\ 510 \ clk = 0, \ C = \\ 520 \ clk = 1, \ C = \\ 520 \ clk = 1, \ C = \\ 520 \ clk = 1, \ C = \\ 530 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 530 \ clk = 0, \ C = \\ 535 \ clk = 1, \ C = \\ 540 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 550 \ clk = 0, \ C = \\ 555 \ clk = 1, \ C = \\ 560 \ clk = 0, \ C = \\ 566 \ clk = 1, \ C = \\ 566 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 576 \ clk = 1, \ C = \\ 586 \ clk = 1, \ C = \\ 586 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 596 \ clk = 1, \ C = \\ 600 \ clk = 0, \ C = \\ 605 \ clk = 1, \ C = \\ 606 \ clk = 1, \ C = \\ 610 \ clk = 0, \ C = \\ 615 \ clk = 1, \ C = \\ 616 \ clk = 1, \ C = \\ 620 \ clk = 0, \ C = \\ 625 \ clk = 1, \ C = \\ 630 \ clk = 0, $	<pre>1100000011111111, 11000000000000000, 0100000000</pre>	Halt = 0 Halt = 1 Halt = 0 Halt = 0	

...But as the multiplier is supposed to disable its output when the result is not ready, I changed a little the test file to do it (by setting CEz at 1 when the device is busy, which place C in a high impedance state).

```
Systolic_multiplier_test.v
                                                                         _ 0
             module Systolic_multiplier_test;
      1
      2
                    reg [7:0] A, B;
      3
                    reg Im,Resetz,CEz,clk;
      4
      5
                    wire [15:0] C;
      6
                    wire Halt;
      7
             Systolic_multiplier inst(C, Halt, A, B, Im, Resetz, CEz, clk);
      8
      9
     10
             initial begin
             $monitor($time, " clk = %b, C = %b, Halt = %b", clk, C, Halt);
     11
     12
     13
                    clk = 0;
     14
                    Im = 1;
     15
                    CEz = 1;
     16
                    Resetz = 1;
     17
                    A = -127;
     18
     19
                    B = -127;
                                      // result expected : 3F01
     20
                    #1 Resetz = 0;
     21
                    #1 Resetz = 1;
     22
                    @(Halt) CEz = 0;
     23
                    #9 CEz = 1;
     24
     25
                    Im = 0;
                    B = 127;
                                      // result expected : COFF
     26
     27
                    #1 Resetz = 0;
                    #1 Resetz = 1;
     28
     29
                    Q(Halt) CEz = 0;
                    #9 CEz = 1;
     30
     31
                    Im = 1;
     32
                    A = 127;
     33
                    B = -127;
     34
                                      // result expected : COFF
     35
                    #1 Resetz = 0;
                    #1 Resetz = 1;
     36
     37
                    @(Halt) CEz = 0;
     38
                    #9 CEz = 1;
     39
     40
                    Im = 0;
                    B = 127;
                                      // result expected : 3F01
     41
     42
                    #1 Resetz = 0;
                    #1 Resetz = 1;
     43
     44
                    //wait(Halt);
                    @(Halt) CEz = 0;
     45
                    #9 $finish;
     46
     47
             end
     48
     49
             always #5 clk = ~clk;
     50
             endmodule
```

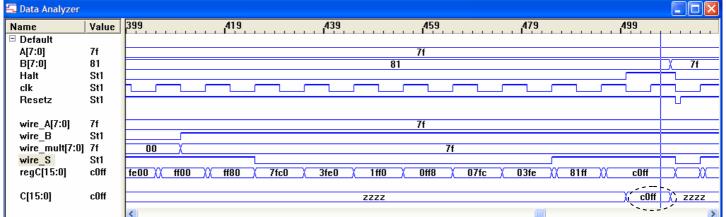
Chronogram result for 1^{st} multiplication: $-127 \times -127 = 16129$ (= $0x81 \times 0x81 = 0x3F01$)



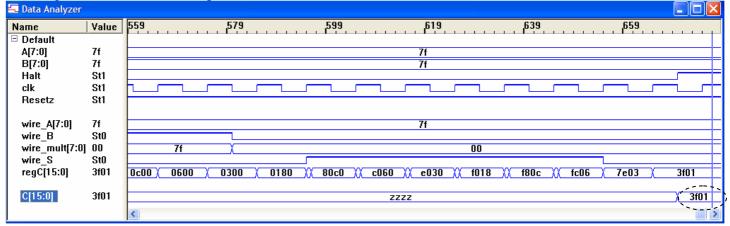
Chronogram result for 2^{nd} multiplication: $-127 \times 127 = -16129$ (= $0x81 \times 0x7F = 0xC0FF$)

🚾 Data Analyzer			
Name	Value	233 253 273 293 313 333	
🖻 Default			
A[7:0]	81	81	7 f
B[7:0]	7f	7f	81
Halt	St1		
clk	St1		
Resetz	St1		
wire_A[7:0]	81	81	7 f
wire_B	St0		
wire_mult[7:0]		81 (00	<u>(7f)</u>
wire_S	St1		
regC[15:0]	cOff	X ff00 X ff80 X 7fc0 X 3fe0 X 1ff0 X 0ff8 X 07fc X 03fe X 81ff X c0ff	(<u>) () () () () () () () () () () () () ()</u>
			` \
C[15:0]	cOff	ZZZZ COff	zzzz
			>

Chronogram result for 3^{rd} multiplication: $127 \times -127 = -16129$ (= $0x7F \times 0x81 = 0xC0FF$)



Chronogram result for 4th multiplication: $127 \times 127 = 16129$ (=0x7F × 0x7F = 0x3F01)



2 Gate level multiplier

Now we have seen that the Verilog design is efficient. We are thus going to stick to its principle but all the virtual time management of Silos becomes sometime a little more complex in gate level considering that all the gate delays are not zero and all the behavioural description are not always easy to translate (synthesize).

"RegA" block diagram:

24 loadA Clk VCC 26 Clk 27 A[81] VCC	A1 02 A2 02 A3 02 A4 02 A4 02 D3 A4 02 D3 A6 02 D5 D6 D7 D6 D7 D7 D8 D8 D8 D8 D8 D8 D8 D8 D8 D8	Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8	wire A1 wire A2 wire A3 wire A4 wire A5 wire A6 wire A7 wire A8
<u>gutput</u> wire_A[81]	CLK CLRN PRN		

"RegA" test chronogram:

	e ennomogra									
Name:	Value:	100.0us 2	00.0us	300.0us	400.0us	500.0us	600.0us	700.0us	800.0us	900.0us
IoadA	T o 1									
■ A[81]	B 01100110	0000000		χ			0110011	0		
wire_A[81]	B 00000000	00	000000) (01100110		

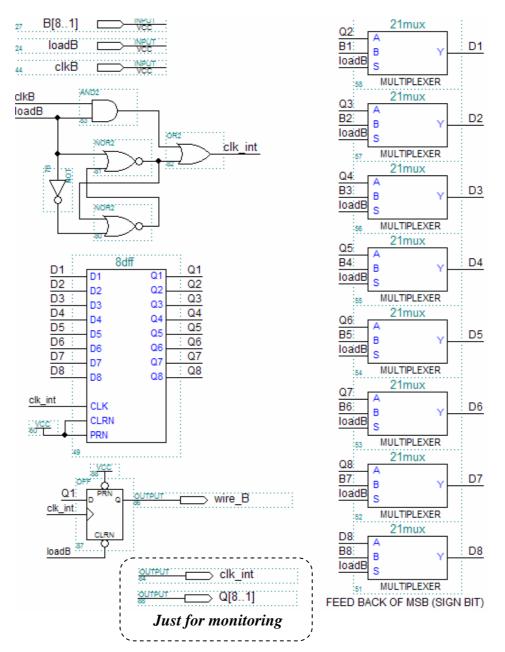
The result expected is obtained: at the clock edge we get the input in output.

"RegA" time analysis:

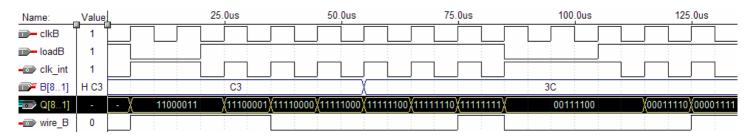
			D	elay Mat Destination	rix			
	wire_A1	wire_A2	wire_A3	wire_A4	wire_A5	wire_A6	wire_A7	wire_A8
A1								
A2								
A3								
A4								
A5								
A6								
A7								
A8								
loadA	6.5ns	6.5ns	6.5ns	6.5ns	6.5ns	6.5ns	6.5ns	6.5ns
			0	50	100	1		
						•		

We keep these results for later, to see the speed limit of our final component.

"b_piso" block diagram: (parallel in serial out)



"b_piso" test chronogram:



Note: as we can see, I've added 2 extra outputs to be able to monitoring the DFF values and the internal clock (clk_int). The sign Bit is correctly propagated and the output of the module is the LSB as wanted.

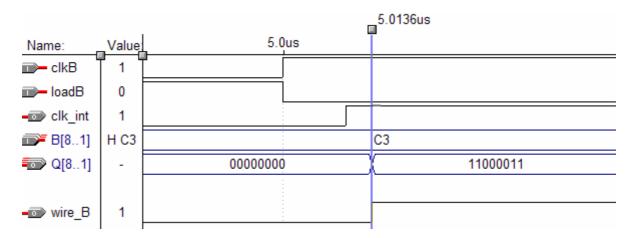
The internal clock was not a piece of cake to create, it seems to be simple but it's a RS flip flop connected with another logical bloc that allows to disable the clock when it's loading.

"b_piso" time analysis: for some reason the analyser doesn't want to simulate this component:

🖄 Timing Analyz	zer 📃	
	Delay Matrix	_
MAX+pl	us II - Timing Analyzer	
S o u r c e	No valid source nodes are tagged for the current timing analysis mode	
	0 <u>50</u> 100	
	Stort Stop List Paths	

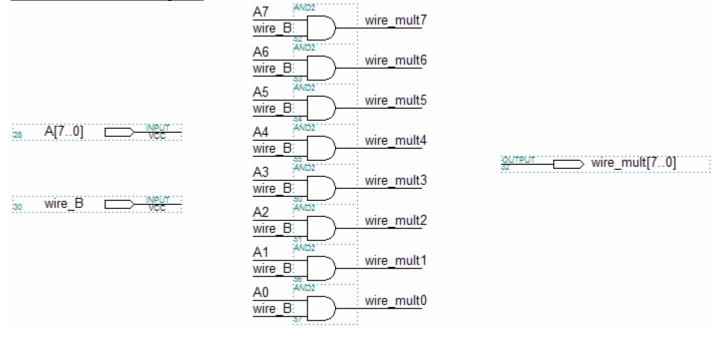
...but nothing can stop me!

=> I zoomed (a lot) on all transitions of the "b_piso" test chronogram and I found the longest time delay:



It thus seems that the longest time delay is 13.6ns

"REG_mult" block diagram:



"REG_mult" test chronogram:

Name:	Value:	100.	0us 200.(0us 300.0u	ıs 400.0us	500.0us	600.0us	700.0us	800.0us	900.0us	1.0
im≱ A[70]	В 0000000	-) (11111111		0000	0000	(11001100		
— wire_B	1										
wire_mult[70]	B 00000000	00000000	<u>11111111)</u>		00000	00		<u>)</u> 11001	1100 🗴 00000	000 🚶 110	01100

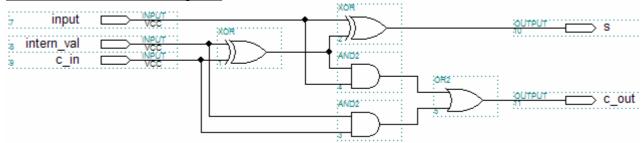
Note: This component, completely combinatorial, is definitely the simplest of the multiplier, but the paradox is that it's the only one to perform a real multiplication!

"REG_mult" time analysis

			D	elay Mat	rix			
	wire_mult0	wire_mult1	wire_mult2	wire_mult3	wire_mult4	wire_mult5	wire_mult6	wire_mult7
A0	6.0ns							
A1		6.0ns						
A2			6.0ns					
A3				6.0ns				
A4					6.0ns			
A5						6.0ns		
A6							6.0ns	
A7								6.0ns
wire_B	6.0ns							
			0	50	100			

As explained in the Verilog design, to make the sum, I used a full adder and I've duplicated it with synchronised feed back of the carry (by a DFF).

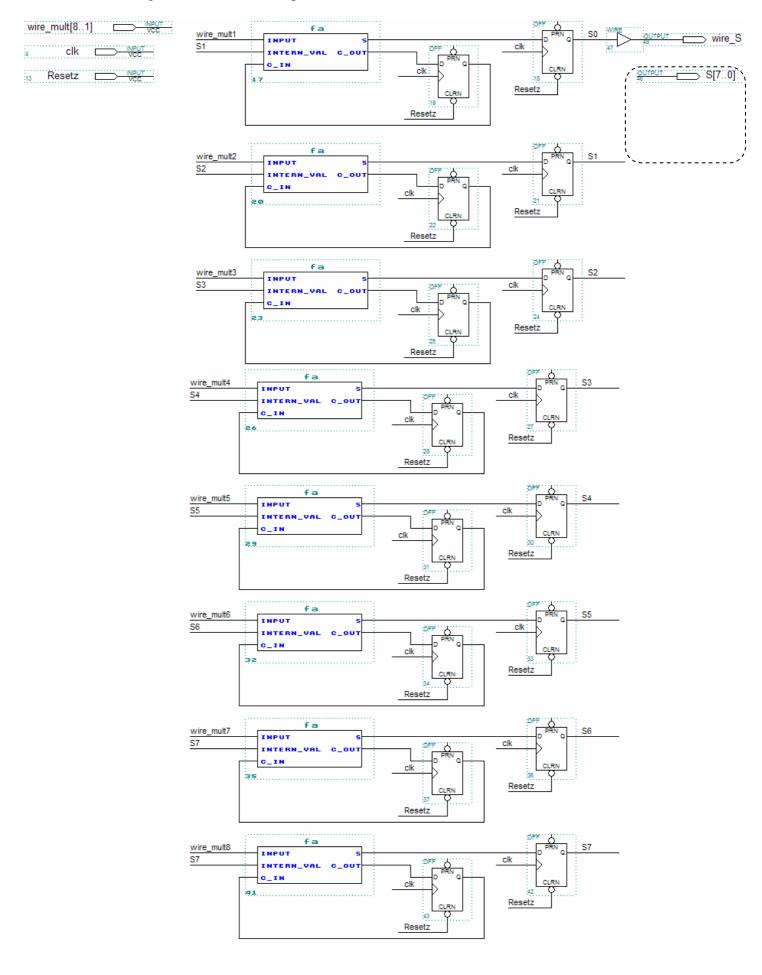
"fa" (Full Adder) block diagram:



"fa" (Full Adder) time analysis:

2	Timing Analyze	er	
	De	elay Mat	rix 🔒
		Destination	
		c_out	S
S	c_in	6.0ns	6.0ns
o u	input	6.0ns	6.0ns
г	intern_val	6.0ns	6.0ns
c e			-
•			Þ
ſ	0	50	100
14			
	<u>S</u> tart	Stop	List Paths

"summ" block diagram: (here is the component that effectuate the instantiation of the full adder)

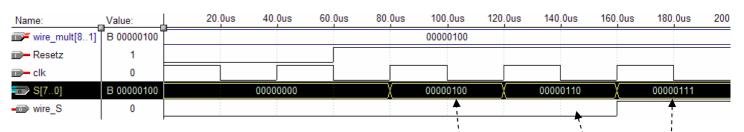


"fa" (Full Adder) test chronogram:

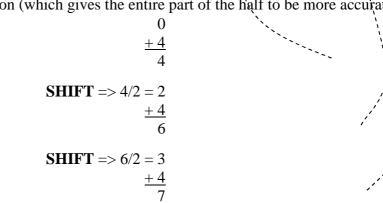
Name:	Value:	L 10.	0us 20.	Ous 30.	0us 40.	.0us 50.	0us 60.	0us 70.	0us 80
intern_val	[0 ¹					<u> </u>			
input	0				- - - -				
<mark>m─</mark> ─ c_in	1				j				
- c_out	0					1			
- 0 s	1					<u></u>			
🗊 inputs	B 001	000	001	010	011	100	(101)	110	111
🖘 sum of inputs	D 1	0	1	1	2	(1	2	2	3

To try making the test more readable I used the "group" function that allows taking several pins to make a bus. I displayed the value of the inputs in binary to see the number of "1" in the bus created and in output, the display is in decimal to se the result directly.

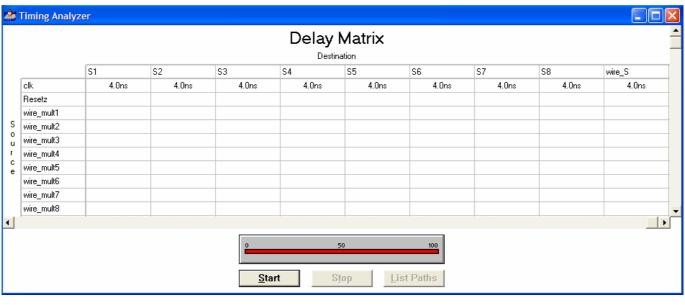
"summ" test chronogram:



In the extra output called "S" we obtain *half* of the sum of the input "wire_mult" and the previous "S" state. => *half* because of the **shift** action (which gives the entire part of the half to be more accurate). We thus obtain as expected: 0

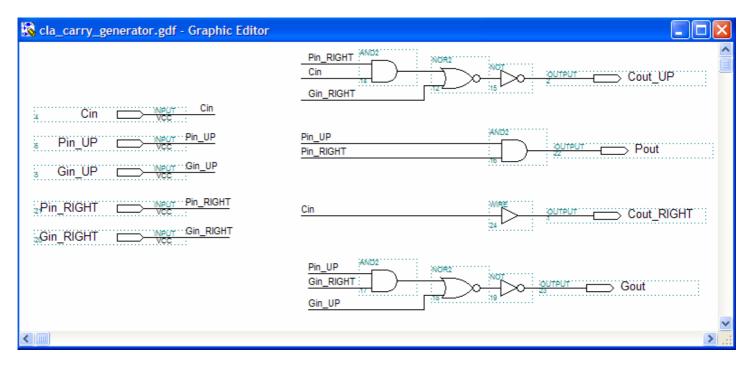


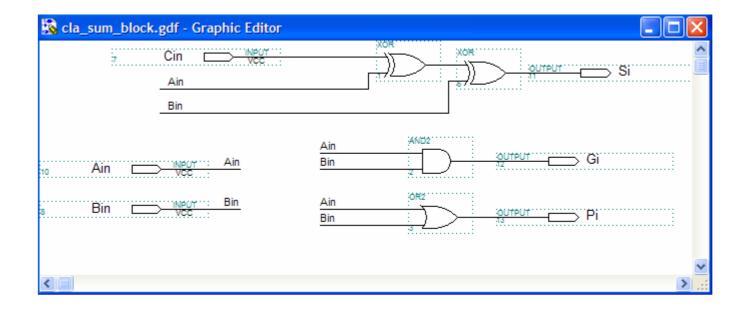
. . .



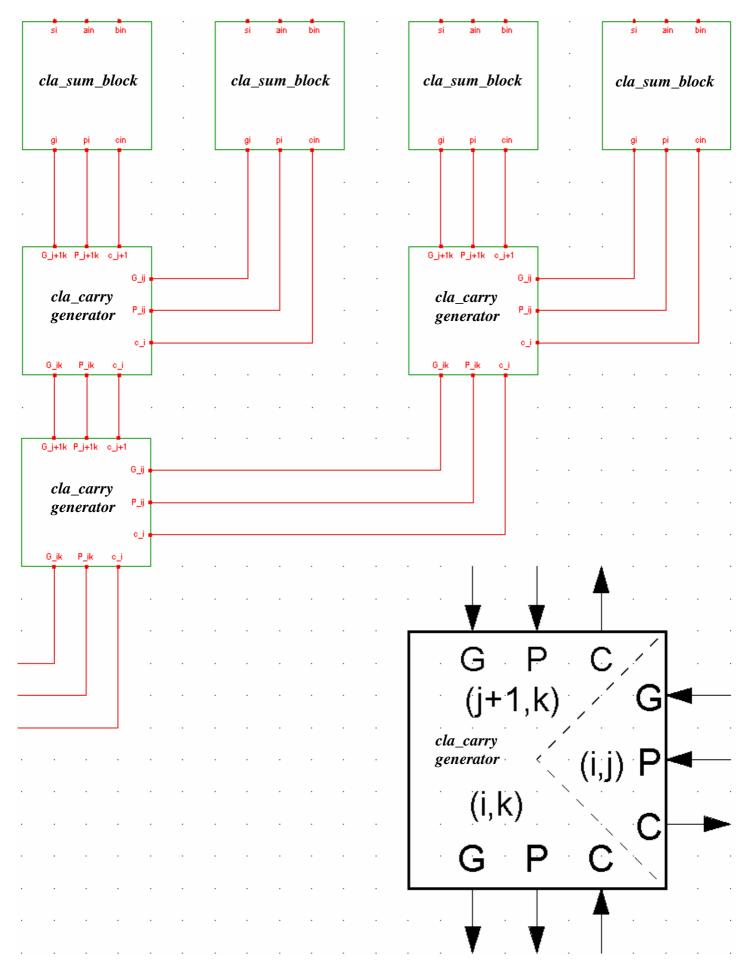
" summ " time analysis:

I've had the idea to use a Carry-Look-Ahead adder before I've chosen this design (to go quicker). In my 1st shot have not thought that the carry can be "sequentially rippled" then doesn't take that much time! ...however, the CLA adder was really complex and didn't allow saving a lot of time, it's just interesting from more than 16bits additions. But I've implemented (in a long night) then I show it, for the souvenir:



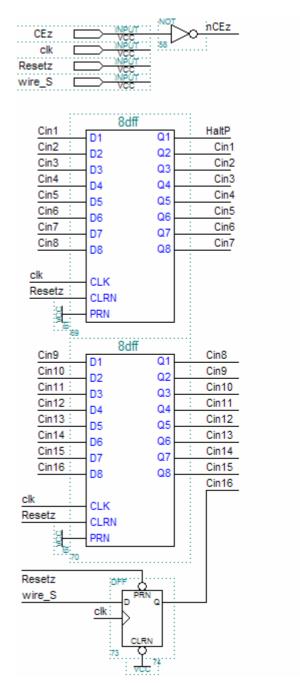


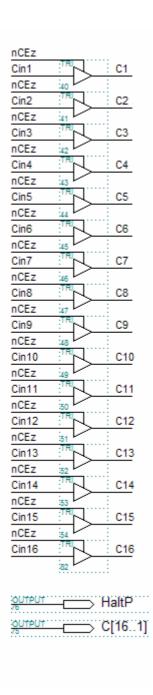
Here is a part of the CLA adder design (just for 4 bits) but the tree is just doubled.



source: http://tams-www.informatik.uni-hamburg.de

"C_SIPO" block diagram: (serial in parallel out)





This component allows implementing the high impedance state by using the tristate gate, it also allows resetting with the MSB at 1 (it's the marker that will count the 16 clock edges to raise the halt signal when the multiplication is finished) and finally it contains the halt memory cell.

"C_SIPO" test chronogram:

Just to show h	10 it works	s I've se	t the signal	CEz at 1 to p	place the out	tput in high ii	npedance st	tate	
Just to show h	Value:		25.0us	50.0us	75.0us	100.0us	125.0us	150.0us	175.0us
wire_S	0	-							
🗩 Resetz	1								
EEz	0								<u>```</u>
m ⊢ clk	1								
- 💿 C16	1								
- 💿 C15	0								
- C 14	0								
- C13	0								
- C12	0								
-🗊 C11	0								
- C10	0								
- 💿 C9	0								
- 💽 C8	0								
-@ C7	0								
-@ C6	0								
- 🗊 C5	0								
- 🗊 C4	0								
-@ C3	0								
-@ C2	0								
- C1	0								
- HaltP	0								``

...and we can see the halt signal raised at the 16^{th} clock edges.

"C_SIPO " time analysis:

					Delay	Matrix					
					Desti						
	C1	C2	C	3	C4	C5	C6	C7		C8	C9
z		5.2ns	5.2ns	5.2ns	5.2ns	5.2ns	5.2	ns	5.2ns	5.2ns	5.2ns
<		4.0ns	4.0ns	4.0ns	4.0ns	4.0ns	4.0	ns	4.0ns	4.0ns	4.0ns
esetz											
re_S											
						50					
				0		50	100				
				<u>S</u> tart	5	top <u>I</u>	ist Paths				
						Tob 1 1	in a survey of the second seco				
						<u>70</u> b					
2	Timing Anal	yzer				τοb Τ					
:	Timing Anal	yzer									
	Timing Anal	yzer			Delay	Matrix					
	Timing Anal				Delay	Matrix					
		C10	C11	C12	Delay Destii	Matrix nation C14		C15	C16	Halt	
s	CEz		C11 5.2ns	C12	Delay Destii	Matrix		C15 5.2ns	C16		P
	CE z clk	C10		C12 \$ 5.2	Delay Desti C13	Matrix nation C14				ns	
S o u r	CEz clk Resetz	C10 5.2ns	5.2ns	C12 \$ 5.2	Delay Desti C13	Matrix nation 5.2ns	5.2ns	5.2ns	5.2	ns	P
S o u	CE z clk	C10 5.2ns	5.2ns	C12 \$ 5.2	Delay Desti C13	Matrix nation 5.2ns	5.2ns	5.2ns	5.2	ns	P
S o u r c	CEz clk Resetz	C10 5.2ns	5.2ns	C12 \$ 5.2	Delay Desti C13	Matrix nation 5.2ns	5.2ns	5.2ns	5.2	ns	₽ 4.0ns
S o u r c e	CEz clk Resetz	C10 5.2ns	5.2ns	C12 s 5.2 s 4.0	Delay Destii C13 18 18	Matrix nation 5.2ns 4.0ns	5.2ns 4.0ns	5.2ns	5.2	ns	P
S o u r c e	CEz clk Resetz	C10 5.2ns	5.2ns	C12 \$ 5.2	Delay Destii C13 18 18	Matrix nation 5.2ns	5.2ns	5.2ns	5.2	ns	P

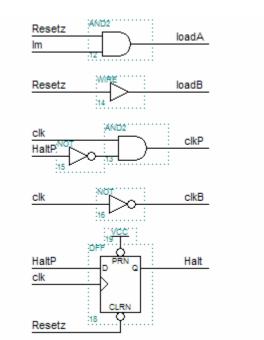
"CNTR" block diagram: (control unit)

Resetz

clk

lm

HaltP

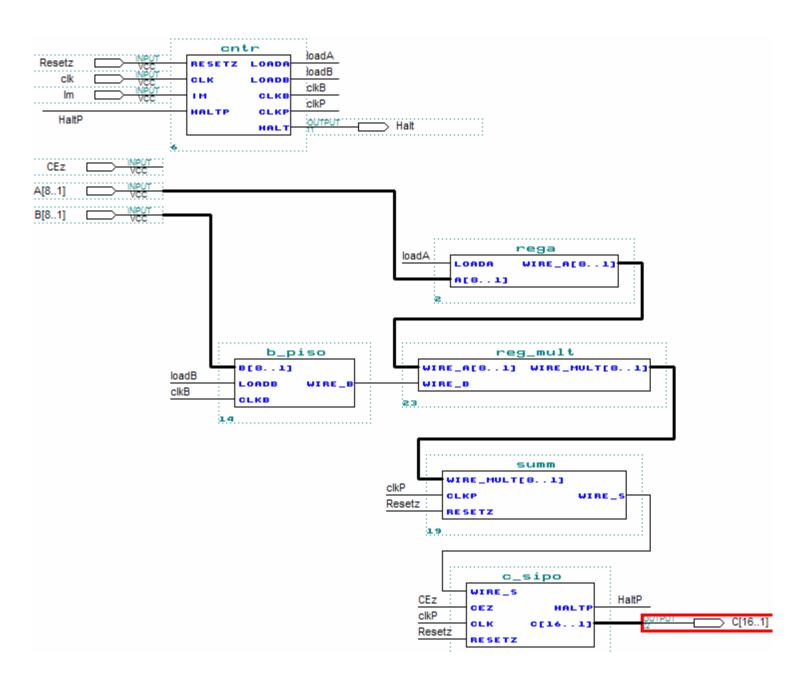


OUTPUT	loadA
	loadB
	clkB
	clkP
	📥 Halt

"CNTR" time analysis:

		Delay N Destina			
	clkB	clkP	Halt	loadA	loadB
clk	6.0ns	6.0ns	4.0ns		
HaltP		6.0ns			
lm				6.0ns	
Resetz				6.0ns	6.0ns
					•
	0	50)	100	
	<u>S</u> tar	t St	op <u>L</u> ist	Paths	

"Systolic multiplier" block diagram: (instantiation of all the components)



"Systolic multiplier" time analysis:

						elay Mat							
		C1	C2	C3	C4	C5		C6	C7		C8		C9
I													
2													
3													
1													
5													
6													
7													
3													
-													
2													
3													
1 -													
5													
6 7													
3													
s Ez		5.5ns	5.5ns	5.5ns	5	5ns	5.5ns	5.5ns	5	.5ns	5.5		5.5ns
-2 k		7.5ns/12.5ns	7.5ns/12.5ns	7.5ns/12.			ns/12.5ns	7.5ns/12.5		:/12.5ns	7.5ns/*		7.5ns/12.
ν I		7.018712.018	7.008712.008	7.008712.	uns 7.0ns	712.008 7.0	18712.008	7.018712.0	is 7.5hs	712.008	7.0087	12.0ns	7.008712.
esetz													
JUDIL													
2	Timing	Analyzer			Start	50 S <u>t</u> op		t Paths					
	Timing	Analyzer				Stop elay Mat						(
	Timing		611		De	Stop	rix	t Paths		610			
		Analyzer C10	C11		De	Stop elay Mat				C16		Halt	
	A1		C11		De	Stop	rix	t Paths		C16			
	A1 A2		C11		De	Stop	rix	t Paths		C16			
	A1 A2 A3		C11		De	Stop	rix	t Paths		C16			
	A1 A2 A3 A4		C11		De	Stop	rix	t Paths		C16			
	A1 A2 A3 A4 A5		C11		De	Stop	rix	t Paths		C16			
	A1 A2 A3 A4		C11		De	Stop	rix	t Paths		C16			
	A1 A2 A3 A4 A5 A6		C11		De	Stop	rix	t Paths		C16 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2			
S	A1 A2 A3 A4 A5 A6 A7		C11 		De	Stop	rix	t Paths		C16 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2			
	A1 A2 A3 A4 A5 A6 A7 A8		C11 		De	Stop	rix	t Paths		C16 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2			
S o u r	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3		C11 		De	Stop	rix	t Paths		C16 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2			
S 0 1	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3 B4		C11 		De	Stop	rix	t Paths		C16			
Sourc	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3 B4 B5		C11 		De	Stop	rix	t Paths		C16 			
Sourc	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3 B4 B5 B6		C11 		De	Stop	rix	t Paths		C16 C16 C16 C16 C16 C16 C16 C16			
Sourc	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3 B4 B5 B6 B7		C11 		De	Stop	rix	t Paths		C16 C16 			
Sourc	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3 B4 B5 B6 B7 B8	C10 			2 2	Stop	rix C14 C14 C14 C14 C14 C14 C14 C14	t Paths t Paths C19 C19 C19 C19 C19 C19 C19 C1					
Sourc	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3 B4 B5 B6 B7 B8 CEz	C10 	5ns	C1	2 2 5.5ns	Stop	ri× C14	E Paths E Paths C18 C18 C18 C18 C18 C18 C18 C1	5.5ns	5.5	5ns	Halt	
Sourc	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3 B4 B5 B6 B7 B8 CEz Ck	C10 	5ns	C1	2 2	Stop	ri× C14	t Paths t Paths C11 C11 C11 C11 C11 C11 C11 C	5.5ns 5ns/12.5ns	5.5		Halt	
Sourc	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3 B4 B5 B6 B7 B8 CEz Ck Im	C10 C10 C10 C10 C10 C10 C10 C10	5ns	C1	2 2 5.5ns	Stop	ri× C14	E Paths E Paths C18 C18 C18 C18 C18 C18 C18 C1		5.5	5ns	Halt	5ns
S o u r c e	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3 B4 B5 B6 B7 B8 CEz Ck	C10 C10 C10 C10 C10 C10 C10 C10	5ns	C1	2 2 5.5ns	Stop	ri× C14	E Paths E Paths C18 C18 C18 C18 C18 C18 C18 C1		5.5	5ns	Halt	5ns
Sourc	A1 A2 A3 A4 A5 A6 A7 A8 B1 B2 B3 B4 B5 B6 B7 B8 CEz Ck Im	C10 C10 C10 C10 C10 C10 C10 C10	5ns	C1	2 2 5.5ns	Stop	ri× C14	E Paths E Paths C18 C18 C18 C18 C18 C18 C18 C1		5.5	5ns	Halt	5ns

This analysis seems to give a maximum time of 12.5ns in hot conditions but I found 13.6ns in the component b_piso. The maximum speed is thus around $1/13.6ns \approx 73$ MHz (but this value is just an estimation)

''Systolic multiplier'' chronogram: I used simple values to show the result, for the positive multiplication I display in decimal and for the negative one, I used the hexadecimal display.

Name:	Value:	50.0us	100.0us 15	50.0us 2	200.0us	250.0us	300.0us	350.0us 400
CEz	0							
🗩 Im	1							
🗩 Resetz	1							
🗩 clk	0							
₽ A[81]	D 64				64			
■ F B [81]	D 64				64			
🖅 C[161]	D 0	32768 16384 8192 4	1096 2048 1024 512	256 (128)	64 (32) 1	16 (8 (32772	x16386 8193 x	4096
–🗩 Halt	0							

職 multiplier	🗞 multiplier.scf - Waveform Editor										
Start: 0.0ns		♦ ♦ Er	nd: 400.0u	s	Interval: 400.	Ous			^		
Name:	Value:	50	.0us	100.0us	150.0us	200.0us	250.0us	300.0us	350.0us		
CEz	0										
🗩 Im	1										
n Resetz	1										
📭 clk	0		ЛЛ								
■ A[81]	H FF					FF					
₽ B[81]	H 02					02					
💿 C[161]	H 8000	8000 4000	A000 D00	0 (E800 (F40	0 (FA00 (FD00 (F	E80 FF40 FFA0	FFD0 FFE8 FF	4 FFFA FFFD	FFFE		
🕳 Halt	0										
< -									> .::		

Note: in this report file (*.rpt) we can see, among other things, the element used in the FPGA chip

Logic	Array Block	Logic Cells	1/0 P	ins	Sharea Expand		Exter Interco	
A:	LC1 - LC16	4/16(25%)	12/12(1	00%)	1/16(6%)	6/36(16%)
В:	LC17 - LC32	16/16(100%)	8/12(66%)	3/16(18%)	28/36(77%)
C:	LC33 - LC48	16/16(100%)	4/12(33%)	12/16(75%)	26/36(72%)
D:	LC49 - LC64	16/16(100%)	11/12(91%)	4/16(25%)	20/36(55%)
Total	dedicated inp	ut pins used:			2/4	(50%)	
	I/O pins used	•			35/48	•	72%)	
	logic cells u				52/64	Ċ	81%)	
	shareable exp				4/64	ć	6%)	
Total	Turbo logic c	ells used:			52/64	(81%)	
Total	shareable exp	anders not avai	ilable (n/a):	16/64	(25%)	
Averag	je fan-in:				5.11			
Total	fan-in:				266			
Total	input pins re	quired:			20			
Total	output pins r	equired:			17			
Total	bidirectional	pins required:	:		0			
	logic cells r	•			52			
	flipflops req				50			
	product terms	•			180			
	-	ending paralle	-	lers:	0			
Total	shareable exp	anders in datat	base:		3			

...and we can see the chip selected by Maxplus: (the speed limit depends also on the FPGA selected):

** DEVICE SUMMARY **						
Chip/ POF Device	Input Pins	Output Pins	Bidir Pins	LCs	Shareable Expanders	% Utilized
multiplier EPM7064LC68-7	20	17	0	52	4	81 %
User Pins:	20	17	0			\smile

<u>BONUS</u> : As I still have a few "seconds" before I return this assignment, I've done a simulation of the Verilog code (sometimes modified) in Maxplus.

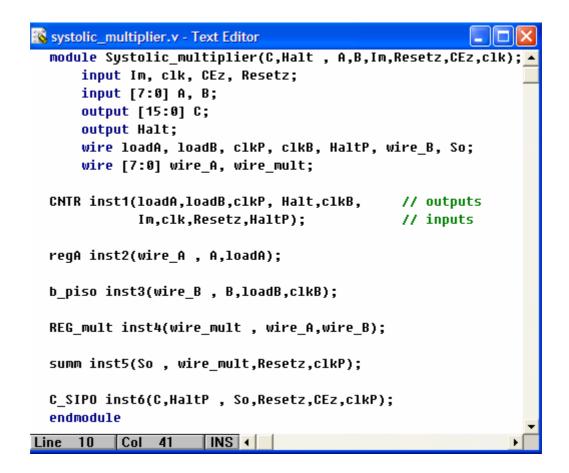
<pre>module regA(wire_A , A,loadA); _ output [7:0] wire A;</pre>	
input [7:0] A;	
input loadA;	
reg [7:0] wire_A;	
always@(negedge loadA)	
wire_A = A;	
endmodule 🗸 🗸	
Line 1 Col 1 INS ()	
🖹 b_piso.v - Text Editor	×
<pre>module b_piso(wire_B, B,loadB,clkB);</pre>	•
output wire_B;	
reg wire_B;	
input [7:0] B;	
input loadB, clkB;	
reg [7:0] B_reg;	
always@(posedge clkB)	
if(~loadB) begin	
B_reg = B;	
wire_B = B_reg[0];	
end	
else begin	
B_reg[6:0] = B_reg[7:1];	
<pre>wire_B = B_reg[0];</pre>	
end	
endmodule	•
Line 1 Col 1 INS 4	

```
💊 reg_mult.v - Text Editor
          module REG_mult(wire_mult, wire_A, wire_B);
              output [7:0] wire_mult;
              input [7:0] wire_A;
              input wire B;
              reg [7:0] wire_mult;
          always @ (wire_B or wire_A)
              wire_mult = wire_B * wire_A;
          endmodule
        Line
             1 Col
                        1
                             INS 🔺
       💊 adder_block.v - Text Editor
         module adder_block(So , mult,Si,Resetz,clkP);
             output So;
             input mult, Si, Resetz, clkP;
             req carry, So;
         always@(posedge clkP)
             if(~Resetz) begin
                 carry = 0;
                 So = 0;
             end
             else if(Resetz)
                 {carry, So} = Si + mult + carry;
         endmodule
      Line
             1
                 Col
                             INS 🔺
                       1
🚳 summ.v - Text Editor
                                                         module summ(wire_S , mult,Resetz,clkP);
      output wire S;
      input [7:0]mult;
      input Resetz, clkP;
      wire [6:0]S_int;
```

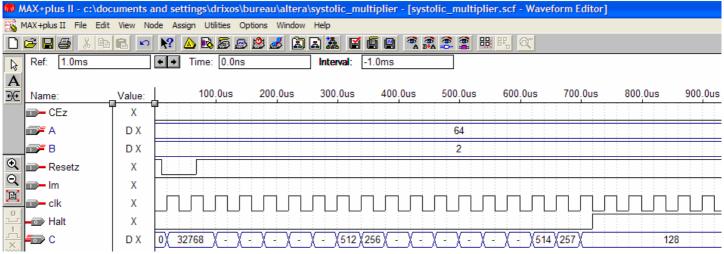
```
adder_block INST0(wire_S, mult[0], S_int[0], Resetz, clkP)
adder_block INST1(S_int[0], mult[1], S_int[1], Resetz, clkP)
adder_block INST2(S_int[1], mult[2], S_int[2], Resetz, clkP)
adder_block INST3(S_int[2], mult[3], S_int[3], Resetz, clkP)
adder_block INST4(S_int[3], mult[4], S_int[4], Resetz, clkP)
adder_block INST5(S_int[4], mult[5], S_int[5], Resetz, clkP)
adder_block INST6(S_int[5], mult[6], S_int[6], Resetz, clkP)
adder_block INST7(S_int[6], mult[7], S_int[6], Resetz, clkP)
endmodule
```

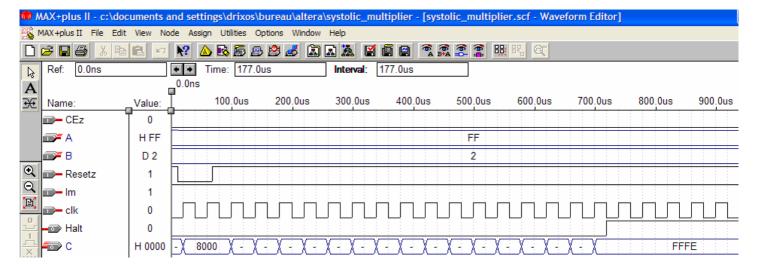
```
💊 c_sipo.v - Text Editor
  module C_SIPO(C , HaltP,wire_S,Resetz,CEz,clkP);
      output [15:0]C;
      output HaltP;
      input wire_S, clkP, Resetz, CEz;
      reg [15:0] C, regC;
      reg HaltP;
  always@(posedge clkP)
  if (~Resetz) begin
      regC = 16'h8000;
      HaltP = 0;
  end
  else begin
      regC = regC>>1;
      #1 regC[15] = wire_S;
      HaltP = regC[0];
  end
  always@(CEz or regC) begin
  if(!CEz)
      C = regC;
  else
      C = 16'hzzz;
  end
Line
          Col
                     INS 🔺
      1
                1
```

```
💫 cntr.v - Text Editor
                                                        module CNTR(loadA, loadB, clkP, Halt, clkB,
                                                  //outputs
            Im, clk, Resetz, HaltP);
                                                  //inputs
  // no more cez ! ! !
      output loadA, loadB, clkP, Halt, clkB;
      input clk, Resetz, Im, HaltP;
      reg Halt, halt_tmp;
  assign loadA = Resetz & Im,
      loadB = Resetz,
      clkP = ~Halt & clk,
      clkB = ~clk;
  always@(posedge clkP) begin
  if (~Resetz) halt tmp = 0;
  else halt_tmp = HaltP;
  end
  always@(negedge clkP) begin
  if (~Resetz) Halt = 0;
  else Halt = halt_tmp;
  end
  endmodule
Line 1 Col 1 INS 🗸
```



SIMPLE EXAMPLE VALUES FOR THE SIMULATION:





** DEVICE SUMMARY **						
Chip/ POF Device	Input Pins	Output Pins	Bidir Pins	LCs	Shareable Expanders	% Utilized
systolic_multiplier EPM7096LC68-7	20	17	0	83	11	86 %
User Pins:	20	17	0			

AS WE CAN SEE THE AUTOMATIC SYNTHESIS FROM VERILOG FILES TAKES MORE PLACE (86% OF THE SAME COMPONENT INSTRAD OF 81)

I'm really happy to have found the time to compare the Verilog synthesis by Maxplus and the gate level synthesis also by Maxplus. This is a good finalisation of the comparison of automatic and manual synthesis. I already knew that the occupation ratio is better in gate level, but now I've seen it for real.

It would have been interesting to test the synthesis size of the behavioural component but time is finished now.

3 Conclusion

This report was a really good approach to the manual synthesis and the gate level fight. The big deal stays in the delay problems, the requirement analysis and the full testing, but we have a good overview of these.

This assignment made me discover a lot of tricks with Maxplus simulator, Silos simulator and also Verilog HDL (definitively confusing considering that I've seen VHSIC HDL last year). However, I have discovered a good overview of these complex uses, but I'm obviously still very far of the full potentials.

My programs are definitively not the only means to reach the aim and obviously, improvements exist but anyway, I'm really proud to have discovered a new design technique and a new HDL, I know it also exists SystemC, A_{ltera} HDL, and more than ten or so but I still have the time...

4 <u>References:</u>

<u>BOOKS</u>: Fundamentals of DIGITAL LOGIC with Verilog design (Brown Vanesic - Mc Graw Hill) DIGITAL FUNDAMENTALS 8th ed. (Thomas FLOYD - Pearson Education International) The Verilog Hardware Description Language 5th ed. (Thomas & Moorby's - Kluwer Academic)

<u>WEBSITES</u>: http://en.wikipedia.org http://www.wordreference.com/fren http://www.cours.polymtl.ca/ele2300/acetates.htm http://ieeexplore.ieee.org http://tams-www.informatik.uni-hamburg.de